الجامعة السعودية الإلكترونية
SAUDI ELECTRONIC UNIVERSITY
2011-1432

College of Computing and Informatics

Digital Logic Design

CS231

Assignment 1

Deadline: Day 03/03/2021 @ 23:59

[Total Mark for this Assignment is 8]

Student Details:

Name: ### **ID:** ###

CRN: ###

Instructions:

- You must submit two separate copies **(one Word file and one PDF file)** using the Assignment Template on Blackboard via the allocated folder. These files **must not be in compressed format**.
- It is your responsibility to check and make sure that you have uploaded both the correct files.
- Zero mark will be given if you try to bypass the SafeAssign (e.g. misspell words, remove spaces between words, hide characters, use different character sets, convert text into image or languages other than English or any kind of manipulation).
- Email submission will not be accepted.
- You are advised to make your work clear and well-presented. This includes filling your information on the cover page.
- You must use this template, failing which will result in zero mark.
- You MUST show all your work, and text must not be converted into an image, unless specified otherwise by the question.
- Late submission will result in ZERO mark.
- The work should be your own, copying from students or other resources will result in ZERO mark.
- Use **Times New Roman** font for all your answers.

Learning Outcome(s):CLO1

Define the concepts, tools, and techniques for the design of digital logic and integrated circuits.

Question One

2.5 Marks

What is the largest 16-bit binary number that can be represented with and justify your answer.

(a) unsigned numbers?

(b) sign/magnitude numbers?

(c) Convert the following hexadecimal numbers to decimal and show your work: $A5_{16}$

(d) Convert the following decimal numbers to unsigned binary numbers. 339_{10}

(e) Perform subtraction on the given binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign. 101010−100111

Learning Outcome(s): CLO1

Concepts, tools and techniques for the design of digital logic and integrated circuits

Question Two

(1.5 Marks)

Simplify these Boolean expressions as much as possible:

a) ((A+D)'(C'+B')'+C)'
b) A'B+CA'D+B'+D'
c) (A+(AB)'+C(AB)')(A+BA'+B')

Learning Outcome(s): CLO2

Develop basic skills of designing combinatorial and sequential logic circuits.

Question Three

3 Marks

Simplify the following Boolean equations using Boolean theorems. Check for correctness using K-map. Draw the logic gates of the simplified equation.

Y = BC+A' B' C'+ BC'

Learning Outcome(s): CLO1

Define the concepts, tools and techniques for the design of digital logic and integrated circuits

Question Four

[1 Marks]

In detail, explain BCD and discuss the advantages and disadvantages of it.

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Assignment 2

Deadline: Sunday 14/11/2021 @ 23:59

[Total Mark for this Assignment is 5]

Student Details:

Name: ### **ID:** ###

CRN: ###

Instructions:

- You must submit two separate copies **(one Word file and one PDF file)** using the Assignment Template on Blackboard via the allocated folder. These files **must not be in compressed format**.
- It is your responsibility to check and make sure that you have uploaded both the correct files.
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- You MUST show all your work, and text must not be converted into an image, unless specified otherwise by the question.
- Late submission will result in ZERO mark.
- The work should be your own, copying from students or other resources will result in ZERO mark.
- Use **Times New Roman** font for all your answers.

Learning Outcome(s): LO1

Define the concepts, tools, and techniques for the design of digital logic and integrated circuits.

Question One

1.5 Mark

Implement the following Boolean function F, together with the don't-care conditions d. Use minimum number of NAND gates for your implementation.

F(A,B,C,D) = Π (5,6,7,11,13,15)
d(A,B,C,D) = Σ(0,2,9,14)

Answer :

This Π is POS form mean grouping the zeros

A B C D Equal in order 8 , 4 , 2 , 1 in numbering the cells

CD \ AB	00	01	11	10
00	X 0	0 4	0 12	0 8
01	0 1	1 5	1 13	X 9
11	0 3	1 7	1 15	1 11
10	X 2	1 6	X 14	0 10

From red group we find terms

A' B'

From green group we find terms

B' D'

From blue group we find terms

C ' D'

So F = A'B' + B'D' + C'D'

or taking complement in POS form (C+D) . (A+B) . (B+D)

Learning Outcome(s): LO1

Define the concepts, tools, and techniques for the design of digital logic and integrated circuits.

1.5 Marks

Question Two

Use K-map to simplify the following expression with don't care conditions producing the least number of terms and literals, then draw the final logic diagram (you can use https://circuitverse.org/simulator for the drawing)

F (w, x, y, z) = ∑ (0, 2, 4, 7, 10, 12), d (w, x, y, z) = ∑ (6, 8)

Answer:

This Σ "Sigma" is SOP form mean grouping the ones

YZ \ WX	00	01	11	10
00	1 (0)	1 (4)	1 (12)	X (8)
01	0 (1)	0 (5)	0 (13)	0 (9)
11	0 (3)	1 (7)	0 (15)	0 (11)
10	1 (2)	X (6)	0 (14)	1 (10)

From red group we find terms

Y'Z'

From Green group we find terms

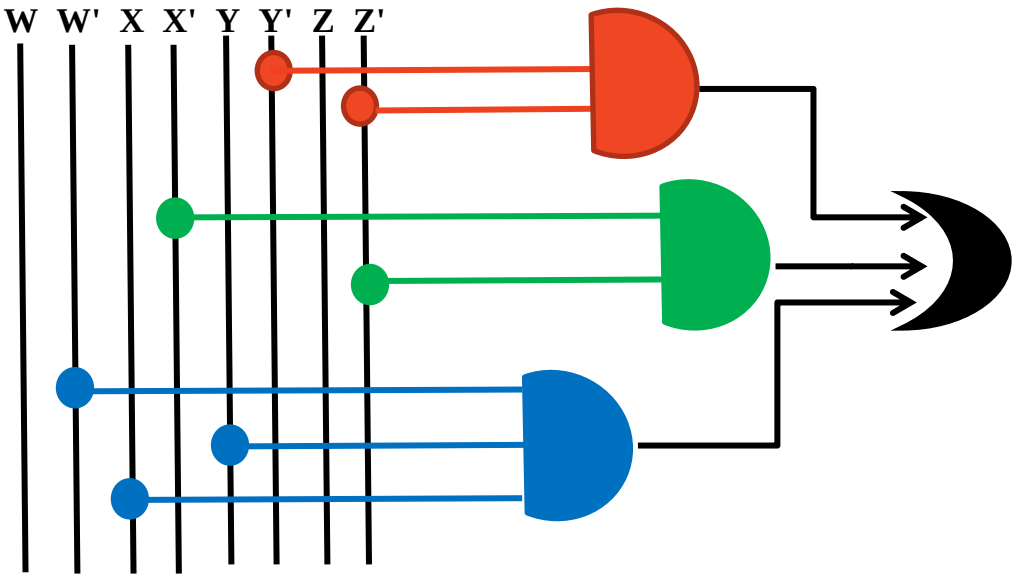
X'Z'

From Blue group we find terms

W'XY

F(W,X,Y,Z) = Y'Z' + X'Z' + W'XY

In Diagram



Learning Outcome(s): 02

Develop basic skills of designing combinatorial and sequential logic circuits.

04

Interpret combinational logic circuits, sequential logic circuits, register transfers, and memory and its related components as the building blocks for digital design.

[2 Marks]

Question Three

Design a combinational circuit with a 3 digits binary input (representing the decimal numbers 0 – 7) and 3 digits binary output. When the binary input is equivalent to the numbers 0, 1, 2 the binary output should represent the same number +1, when the input is 3 or 4 the output should be 0, when the input is 5, 6, 7 the output should be the number -1. (ex. If the input is 1 the output should be 2 if the input is 4 the output is 0 if the input is 7 the output is 6 all in binary format)

Follow the design process

- Give names to input/output
- Make a truth table with the relationship between the input and output
- Use k-map to get the simplified expression for each output

Answer:

	Input			Output		
decimal	**X**	**Y**	**Z**	**A**	**B**	**C**
0	**0**	**0**	**0**	**0**	**0**	**1**
1	**0**	**0**	**1**	**0**	**1**	**0**
2	**0**	**1**	**0**	**0**	**1**	**1**
3	**0**	**1**	**1**	**0**	**0**	**0**
4	**1**	**0**	**0**	**0**	**0**	**0**
5	**1**	**0**	**1**	**1**	**0**	**0**
6	**1**	**1**	**0**	**1**	**0**	**1**
7	**1**	**1**	**1**	**1**	**1**	**0**

For output A

X \ yz	00	01	11	10
0	0 (0)	0 (1)	0 (3)	0 (2)
1	0 (4)	1 (5)	1 (7)	1 (6)

From red group we find terms

XZ

From Blue group we find terms

XY

A(X,Y,Z) = XZ + XY

For output B

X \ yz	00	01	11	10
0	0 (0)	1 (1)	0 (3)	1 (2)
1	0 (4)	0 (5)	1 (7)	0 (6)

From red group we find terms

X' Y' Z

From Blue group we find terms

X' Y Z'

From Green group we find terms

X Y Z

B(X,Y,Z) = X'Y'Z + X'YZ' + XYZ

For output C

X \ yz	00	01	11	10
0	1 0	0 1	0 3	1 2
1	0 4	0 5	0 7	1 6

From red group we find terms

Y Z'

From Blue group we find terms

X' Z'

C(X,Y,Z) = YZ' + X'Z'

Ques

[redacted]tional circuit for binary subtracting can be done using Full adders and 2's complements.

False

Follow the Black Box for Full Grade
BEWARE to Check Answers by yourself

الأفضل أن تراجع الأسئلة قبل الاعتماد على اجوبة الأخرين

Sensei

Que[redacted]

[redacted]circuit, the output at any time depends only on the Input value.

○ False

Ques

[redacted]

ns, 3-bits are needed to store one BCD digit.

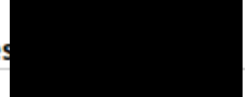
False

Ques

[redacted]

ch can eliminate the indeterminate state of the latch.

Ques



ll always change its stored value when the clock is enabled.

○ False

Ques

[redacted]nal is set to 0 in a decoder the output is affected by the input signal.

○ False

Ques[redacted]

W[redacted]oder to implement logical expression expressed as Minterms we combine the output using _____.

- A combination of AND, OR gates
- A combination of AND, OR NOT gates

Ques[redacted]

W[redacted] a function using the multiplexer, the input to the multiplexers is connected to ether 0 or 1 which represent _____.

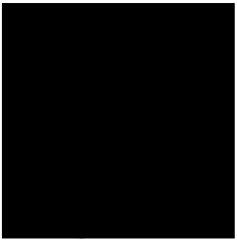
[redacted]e function

[redacted]bles

- The minterms
- The simplified expression values

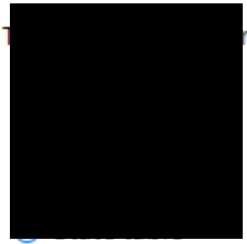
Question 9

The Minterm m2 in a function with 3 variables is expressed as _____.



Question 10

T[redacted]ntains the input, current state, next state, output.



- State input equations

Ques

[redacted]inary number with 2's complement, if there is a carry that means:

[redacted]sitive

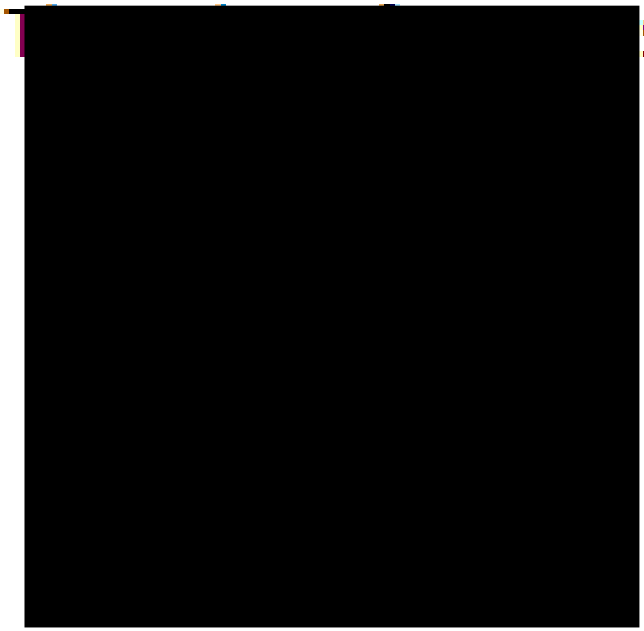
- ○ The result is negative
- ○ Nothing just discards the carry
- ◉ 2's complement

Ques[redacted]

[redacted] inputs of a full adder then the Sum is given by.

- A+B+C
- AB+CB+AC

Question 13


sion (41)10 to binary.

- ○ $(101011)_2$

Question 14

[redacted] base to another first Convert the Integer Part, then Convert the Fraction Part, lastly _____ the two results with radix point.

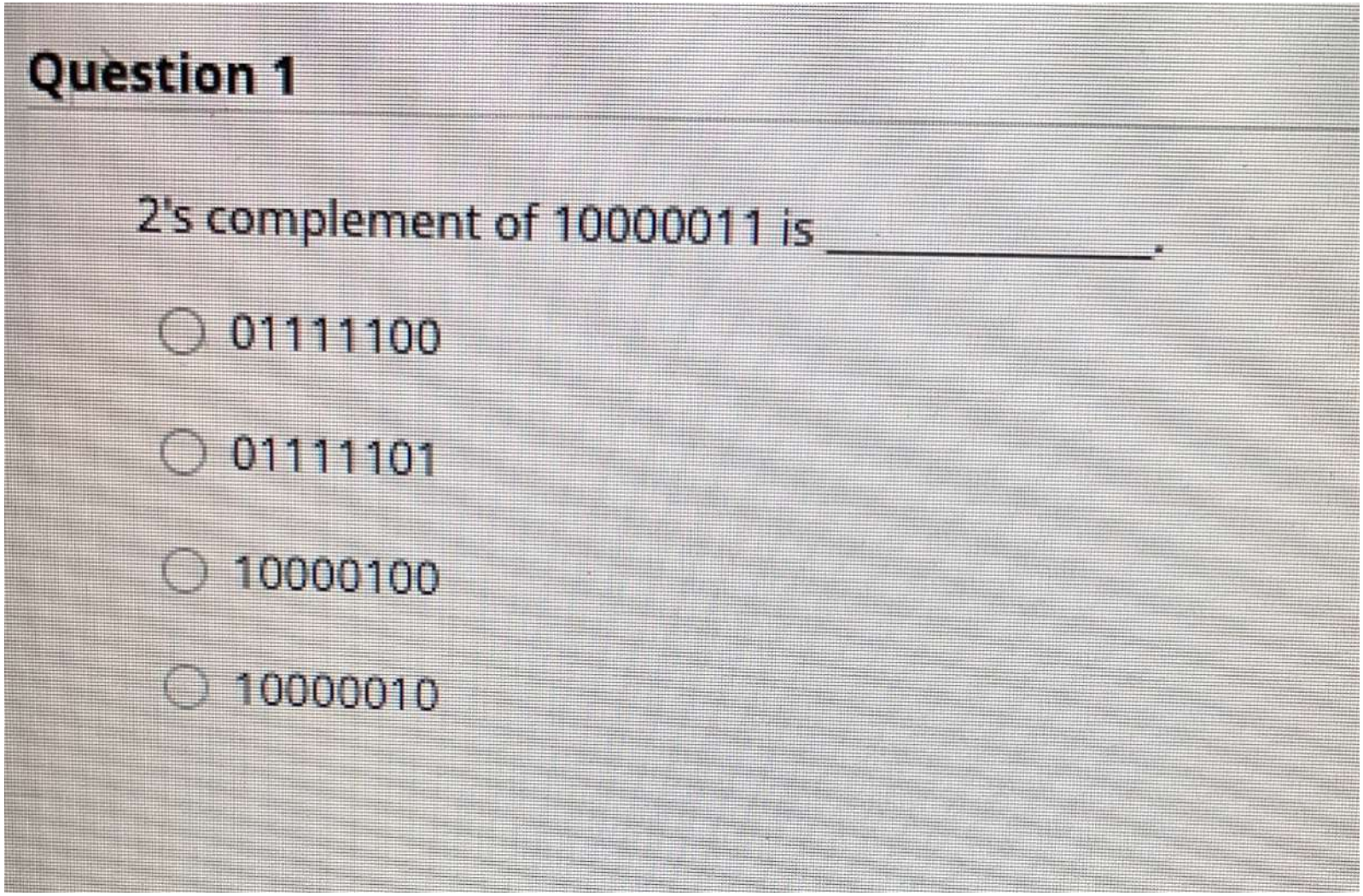
- ○ divide

Ques

[redacted]sists of _____ types of circuits.

- 3
- 4
- 5

This Assignment No answer practice to solve it .. Good Luck



Question 1

2's complement of 10000011 is _____.

- 01111100
- 01111101
- 10000100
- 10000010

In analyzing combinational circuit, we need to make sure that the inputs is not ____

- ○ 1
- ○ Feedback
- ○ 0
- ○ Expression

Question 3

The value of Conversion (41)10 to binary.

- ○ $(11011)_2$
- ○ $(1101)_2$
- ○ $(101001)_2$
- ○ $(101011)_2$

Question 4

A digital system consists of _____ types of circuits.

- ○ 2
- ○ 3
- ○ 4
- ○ 5

Question 5

In magnitude Comparator, to determine whether A is greater or less than B, we inspect the relative magnitudes of pairs of significant digits, starting from the _____.

- ○ Least significant position
- ○ Most significant position
- ○ Decimal conversion
- ○ Value of the Digit

Question 6

In a combinational circuit, the output at any time depends only on the Input value.

- ○ True
- ○ False

⚠ Moving to another question will save this response.

Question 7

In BCD adder, the output sum cannot be greater than 9 + 9.

- ○ True
- ○ False

Question 8

A signal is a physical or virtual quantity that varies with time, or space, or another independent variable. It can be analog or digital signal.

- ○ True
- ○ False

Question 9

If we want to write a truth representing the following equations
F1(x,y,z) = x + x`y + z`
F2 (x,yz) = x`z+ y
We will need :

- 2 rows and 2 columns
- 3 rows and 5 columns
- 3 rows and 3 columns
- 3 rows and 6 columns

Question 10

The _____ is used to determine the next value to be stored in a latch.

- ○ Input equation
- ○ Sequential equation
- ○ State value
- ○ The Q values

Question 11

In combinational logic if we have a circuit with 4 variables for the input and 3 variables for output we can describe _____.

- ○ 4 Boolean equations
- ◉ 3 Boolean equations
- ○ 7 Boolean equations
- ○ 1 Boolean equation

The expression F(A,B,C) = (A`+B+C)(A+B`+C`) is _____.

- ○ Complemented function
- ○ Sum of Minterm
- ○ Product of Maxterms
- ○ Dual function

Question 13

The dual and complement of a function are the same.

- ○ True
- ○ False

Question 14

The order of operation in logical expression evaluation is parenthesis, NOT, AND, OR.

- ○ True
- ○ False

Question 15

Both JK flip-flop and D flip-flop has the option to maintain the current state or change it.

- ○ True
- ○ False

Question 1

In K-map we order the terms based on the binary number order.

- ○ True
- ○ False

Question 2

The regular latch will always change its stored value when the clock is enabled.

- ○ True
- ○ False

Question 3

Both JK flip-flop and D flip-flop has the option to maintain the current state or change it.

- ○ True
- ○ False

Question 4

2's complement of 10000011 is _____.

- ○ 01111100
- ○ 01111101
- ○ 10000100
- ○ 10000010

Question 5

To convert from one base to another first Convert the Integer Part, then Convert the Fraction Part, lastly _____ the two results with radix point.

- ○ sum
- ○ multiply
- ○ join
- ○ divide

Question 6

_____ principle is technique for reducing the carry propagation time in a parallel adder.

- ○ Full Adder
- ○ Carry lookahead logic
- ○ Half Adder
- ○ Propagation Delay

Question 7

A digital system consists of _____ types of circuits.

- ○ 2
- ○ 3
- ○ 4
- ○ 5

Question 8

In analyzing combinational circuit, we need to make sure that the inputs is not _____ .

- ○ 1
- ○ Feedback
- ○ 0
- ○ Expression

Question 9

A register with 4 cells can store any discrete quantity of information that contains 32 bits.

- ○ True
- ○ False

Question 10

Digital signal (Binary) values can be represented only by digits 0 and 1.

- ○ True
- ○ False

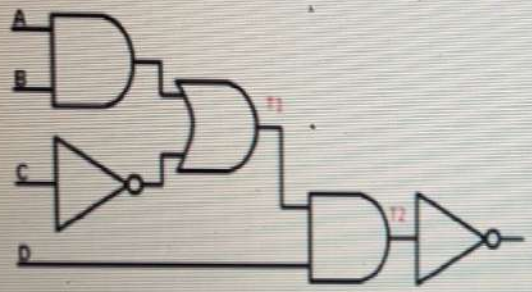
Question 11

Combinational circuit can be analyzed manually by finding the Boolean functions or truth table.

- ○ True
- ○ False

Question 12

In the following circuit diagram what is the intermediate function T1?



- AB+C
- (AB)`+C`
- (AB+C`)(D)
- AB+C`

Question 13

In combinational logic if we have a circuit with 4 variables for the input and 3 variables for output we can describe _____.

- 4 Boolean equations
- 3 Boolean equations
- 7 Boolean equations
- 1 Boolean equation

⚠ Moving to another question will save this response.

Question 14

When using the decoder to implement logical expression expressed as Minterms we combine the output using _____.

- An OR gate
- An AND gate
- A combination of AND, OR gates
- A combination of AND, OR NOT gates

Question 15

When implementing a function using the multiplexer, the input to the multiplexers is connected to ether 0 or 1 which represent _____.

- ○ The values of the function
- ○ The input variables
- ○ The minterms
- ○ The simplified expression values

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Assignment 1

Deadline: Saturday 16/10/2021 @ 23:59

[Total Mark for this Assignment is 5]

Student Details:

Name: ### **ID:** ###

CRN: ###

Instructions:

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- Use **Times New Roman** font for all your answers.

Learning Outcome(s): LO1

Define the concepts, tools, and techniques for the design of digital logic and integrated circuits.

Question One

1,5 Mark

Fill-in the tables below with different representations of a number.

Decimal	Binary	Hexadecimal
154		
		1D.4
0.125		
Addition and Subtracting(with 2's complment)		
(01111111)+ (11011111)	(1010100)− (1000011)	

Answer: [0.25 mark for each operation]

Decimal	Binary	Hexadecimal
154	**10011010**	**9A**
29.25	**00011101.0100**	**1D.4**
0.125	**0.001**	**0.2**
Addition and Subtracting(with 2's complment)		
(01111111)+ (11011111) 01011110	(1010100)− (1000011) 2's complment (0111100)+ (1) 0111101 1010100+ 0111101	

Question One

	10010001 discard carry 0010001	

Learning Outcome(s): LO2

Develop basic skills of designing combinatorial and sequential logic circuits.

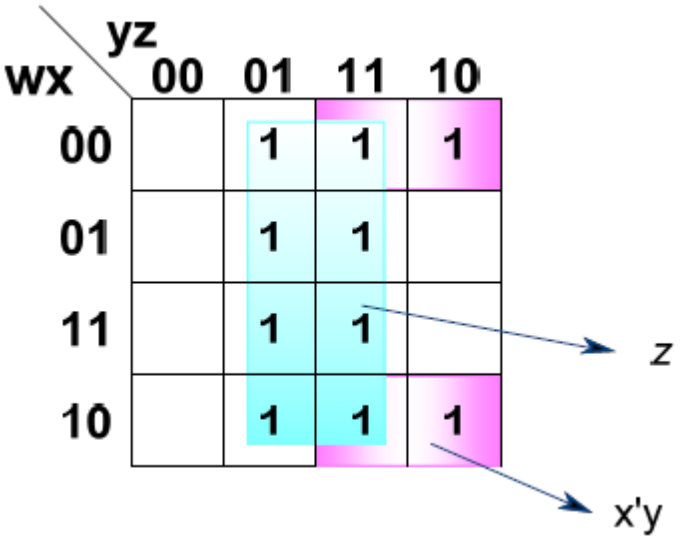
Question Two

[2 Marks]

For the following functions:

a. Simplify Using Karnaugh map then draw the logic gate daigram

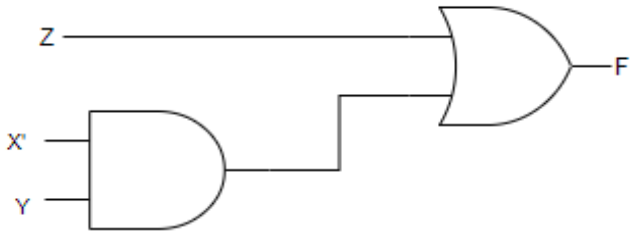
$F(w, x, y, z) = w'z + xz + x'y + wx'z$



Answer:

[0.5 mark for the simplification]

F(w,x,y,z) = Z+X'Y



Question Two

b. Using Boolean Algebraic manipulations, minimize the following functions to minimum number of literals in sum of products representation. Show your work clearly step by step indicating the used properties of Boolean Algebra: $F = (A' + B' + C')(A + C')(B + C')(B' + C)$

First take the dual of F and we get: A' B' C' + A C' + B C' +B' C

= C' [A' B' + A + B] + B'C	by distributive law	[0.25 mark]
= C' [B' + A + B] + B'C	by simplification	[0.25 mark]
= C' [1 + A]+ B'C	by complement	[0.25 mark]
= C' + B'C	by OR identity	[0.25 mark]
= C' + B'	by simplification	[0.25 mark]
Then, we take the dual again, this leads to F4 = B'C'		[0.25 mark]

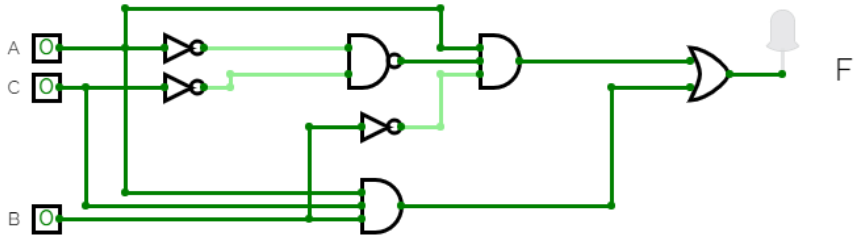
Learning Outcome(s): 02

Develop basic skills of designing combinatorial and sequential logic circuits.

Question Three

1.5 Mark

Generate the truth table from the following digital logic schematic circuit and write the boolean expression for the function F.



Hint: find intermediate values first

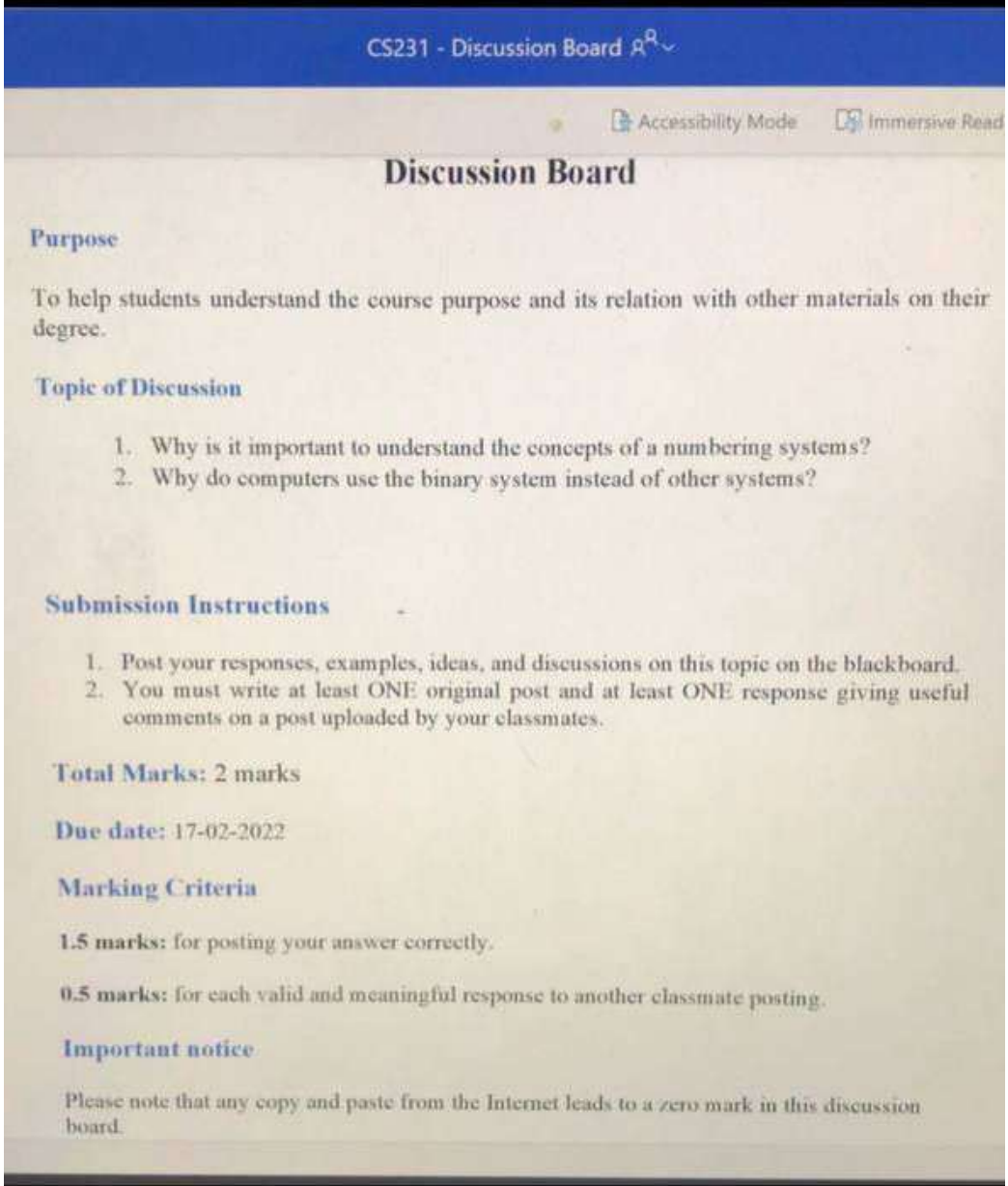
Answer: [Truth table 1 mark (0.125 for each row) and 0.5 mark for the Boolean function F]

									F
A	B	C	A`	B`	C`	$\overline{\bar{A}\cdot\bar{C}}$	$A\cdot B\cdot C$	$A\cdot\overline{\bar{A}\cdot\bar{C}}\cdot\bar{B}$	$A\cdot\overline{\bar{A}\cdot\bar{C}}\cdot\bar{B}+A\cdot B\cdot C$
0	0	0	1	1	1	0	0	0	0
0	0	1	1	1	0	1	0	0	0
0	1	0	1	0	1	0	0	0	0
0	1	1	1	0	0	1	0	0	0
1	0	0	0	1	1	1	0	1	1
1	0	1	0	1	0	1	0	1	1
1	1	0	0	0	1	1	0	0	0
1	1	1	0	0	0	1	1	0	1

$$F = A\cdot\overline{\bar{A}\cdot\bar{C}}\cdot\bar{B}+A\cdot B\cdot C$$

Discussion Board Questions 2 Points Might change

أسئلة الدسكشن بورد من درجتين قد تتغير



Once the quiz is started it **must be completed in a single sitting** and

Best Regards

Instructions	
Timed Test	This test has a time limit of 20 minutes.This test will save and submit automatically when the time expire Warnings appear when **half the time**, **5 minutes**, **1 minute**, and **30 seconds** remain.
Multiple Attempts	Not allowed. This test can only be taken once.
Force Completion	Once started, this test must be completed in one sitting. Do not leave the test before clicking **Save and**
	Your answers are saved automatically.

Remaining Time: 01 minute, 56 seconds.

Question Completion Status:

⚠ Moving to another question will save this response.

Question 21

It is possible to optimize Mux as general purpose logic by finding relation between Function F and one input.

- True
- False

⚠ Moving to another question will save this response.

25°C
سماء صافية

One Attempt only allowed

Once the quiz is started it **must be completed in a single sitting** and within

Best Regards

Instructions	
Timed Test	This test has a time limit of 20 minutes.This test will save and submit automatically when the time expires. Warnings appear when **half the time**, **5 minutes**, **1 minute**, and **30 seconds** remain.
Multiple Attempts	Not allowed. This test can only be taken once.
Force Completion	Once started, this test must be completed in one sitting. Do not leave the test before clicking **Save and Submit**.
	Your answers are saved automatically.

Remaining Time: 01 minute, 37 seconds.

Question Completion Status:

⚠ Moving to another question will save this response.

Question 22

F = A(B + C)(C + D) for such a Boolean expression, The order of evaluation is : Not => Parentheses => AND => OR

- ○ True
- ● False

⚠ Moving to another question will save this response.

	Warnings appear when **half the time**, **5 minutes**, **1 minute**, and **30 sec**
Multiple Attempts	Not allowed. This test can only be taken once.
Force Completion	Once started, this test must be completed in one sitting. Do not leave th
	Your answers are saved automatically.

Remaining Time: 01 minute, 14 seconds.

Question Completion Status:

⚠ Moving to another question will save this response.

Question 23

Invert gate could be performed using 1 NAND gate with the same input.

- ✓ True
- ○ False

⚠ Moving to another question will save this response.

Multiple Attempts Not allowed. This test can only be taken once.

Force Completion Once started, this test must be completed in one sitting. D

Your answers are saved automatically.

Remaining Time: **02 minutes, 45 seconds.**

Question Completion Status:

⚠ Moving to another question will save this response.

Question 18

(X'(YZ)'W')'= (X+Y+W)(X+Z+W)

- True
- False

⚠ Moving to another question will save this response.

25°C
سماء صافية

Esc F1 F2 F3 F4 F5

~ ` ! @ # $ %

ذ 1 ا 2 ٢ 3 ٣ 4 ٤ 5

Once the quiz is started it **must be completed in a single sitting**

Best Regards

Instructions	
Timed Test	This test has a time limit of 20 minutes.This test will save and submit automatically when the time Warnings appear when **half the time**, **5 minutes**, **1 minute**, and **30 seconds** remain.
Multiple Attempts	Not allowed. This test can only be taken once.
Force Completion	Once started, this test must be completed in one sitting. Do not leave the test before clicking **Save** Your answers are saved automatically.

Remaining Time: 03 minutes, 05 seconds.

Question Completion Status:

⚠ Moving to another question will save this response.

Question 17

In binary Subtractor, A-B can be done by taking only the 1's complement of B and adding it to A

- ○ True
- ● False

⚠ Moving to another question will save this response.

25°C
سماء صافية

d Test	This test has a time limit of 20 minutes.This test will save and submit automatically when the time expires. Warnings appear when **half the time**, **5 minutes**, **1 minute**, and **30 seconds** remain.
iple Attempts	Not allowed. This test can only be taken once.
e Completion	Once started, this test must be completed in one sitting. Do not leave the test before clicking **Save and Submit**. Your answers are saved automatically.

maining Time: **59 seconds.**

Less than one minute remains

uestion Completion Status:

⚠ Click **Submit** to complete this assessment.

uestion 24

Storage elements that operate with signal levels are flip flops and the storage elements controlled by a clock transition are Latches

- ○ True
- False

⚠ Click **Submit** to complete this assessment.

Force Completion Once started, this test must be completed in one sitting

Your answers are saved automatically.

Remaining Time: **02 minutes, 27 seconds.**

Question Completion Status:

⚠ Moving to another question will save this response.

Question 19

Boolean algebraic functions use logic operations only

- True
- False

⚠ Moving to another question will save this response.

25°C
سماء صافية

Esc F1 F2 F3 F4 F5

~ ! @ # $ %

Once the quiz is started it **must be completed in a single sit**

Best Regards

Instructions	
Timed Test	This test has a time limit of 20 minutes.This test will save and submit automatically when t Warnings appear when **half the time**, **5 minutes**, **1 minute**, and **30 seconds** remain.
Multiple Attempts	Not allowed. This test can only be taken once.
Force Completion	Once started, this test must be completed in one sitting. Do not leave the test before clicki
	Your answers are saved automatically.

Remaining Time: **02 minutes, 19 seconds.**

Question Completion Status:

⚠ Moving to another question will save this response.

Question 20

In Three variable K map, four adjacent squares represent a term with one literal.

- True
- False

⚠ Moving to another question will save this response.

25°C
سماء صافية

Esc F1 F2 F3 F4 F5 F6

Best Regards

structions	
med Test	This test has a time limit of 20 minutes.This test will save and submit automatically when Warnings appear when **half the time**, **5 minutes**, **1 minute**, and **30 seconds** remain.
Multiple Attempts	Not allowed. This test can only be taken once.
Force Completion	Once started, this test must be completed in one sitting. Do not leave the test before clic Your answers are saved automatically.

Remaining Time: **03 minutes, 56 seconds.**

Question Completion Status:

⚠ Moving to another question will save this response.

Question 13

In a multiplexer, the selection of a particular input line is controlled by selected lines.

- (•) True
- ( ) False

⚠ Moving to another question will save this response.

25°C
سماء صافية

ESC F1 F2 F3 F4 F5 F6

...ining Time: 59 seconds.

uestion Completion Status:

Less than one minute remain

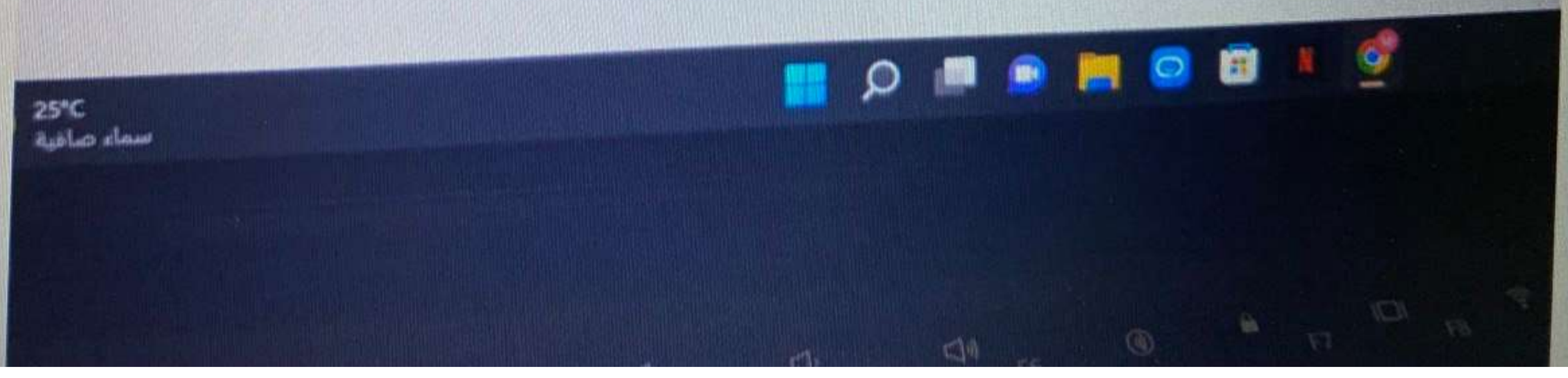
Click **Submit** to complete this assessment.

uestion 24

Storage elements that operate with signal levels are flip flops and the storage elements controlled by a clock transition are Latches

- True
- False

Click **Submit** to complete this assessment.



Moving to another question will save this response.

Question 6

If number of M elements = 34, to represent the element as binary code the minimum number of bits n needed is:

- 5 Bits
- 3 Bits
- 6 Bits
- 4 Bits

Moving to another question will save this response.

25°C
سماء صافية

Esc F1 F2 F3 F4 F5 F6 F7

31°C

Instructions	
Timed Test	This test has a time limit of 20 minutes.This test will save and submit automatic Warnings appear when **half the time**, **5 minutes**, **1 minute**, and **30 seconds** re
Multiple Attempts	Not allowed. This test can only be taken once.
Force Completion	Once started, this test must be completed in one sitting. Do not leave the test be
	Your answers are saved automatically.

Remaining Time: **03 minutes, 43 seconds.**

Question Completion Status:

⚠ Moving to another question will save this response.

Question 14

Gray code uses less power than BCD since it uses less transistors.

- (•) True
- ( ) False

⚠ Moving to another question will save this response.

Your answers are saved automatically.

Remaining Time: 16 minutes, 45 seconds.

Question Completion Status:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

⚠ Moving to another question will save this response.

Question 7 0.25

To obtain POS from K map, by 1. combining the 0 from the map => 2. obtain the Function from the Zeros => Applying DeMorgan theorem on the Function.

- True
- False

⚠ Moving to another question will save this response.

Talk to Cortana

Type here to search

28°C

lenovo

Remaining Time: 17 minutes, 48 seconds.

Question Completion Status:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

⚠ Moving to another question will save this response.

Question 5

feedback paths and memory elements are acceptable in the logic gates diagram of a sequential circuit

- (●) True
- ( ) False

⚠ Moving to another question will save this response.

Type here to search

Lenovo

Your answers are saved automatically.

Remaining Time: 18 minutes, 38 seconds.

Question Completion Status:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	1

⚠ Moving to another question will save this response.

Question 3

For four inputs Multiplexer, 2 Selector bits is needed.

- (●) True
- ( ) False

⚠ Moving to another question will save this response.

Type here to search

Lenovo

Remaining Time: 15 minutes, 28 seconds.

Question Completion Status:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

Moving to another question will save this response.

Question 9

The main difference between half adder and full adder is the existence of carry input as output of full adder.

- ○ True
- ◉ False

Moving to another question will save this response.

Type here to search

Lenovo

Question Completion Status:

1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18

Moving to another question will save this response.

Question 13

4-to-16 Decoder could be used for:

- Convert Binary to Hex
- Select 16-to-1 Output
- Select 8-to-1 Output
- Convert Hex to Binary

Moving to another question will save this response.

Type here to search

Lenovo

⚠ Moving to another question will save this response.

Question 16

Switching function F(A,B,C,D) =A'BCD'+ABCD+A'B'C'D+A'B'CD+ABC'D

- Σ(1, 3, 6, 13, 15)
- Σ(3, 5, 6, 9, 15)
- Σ(2, 4, 7, 10, 11)
- Σ(1, 3 , 5 , 12, 14)

⚠ Moving to another question will save this response.

Remaining Time: 08 minutes, 48 seconds.

Question Completion Status:

Save and Submit

Click **Submit** to complete this assessment.

Question **24** of **24**

Question 24

0.25 points Save Answer

In combinational logic, for 5 input variables there is _____ possible combination of the binary inputs. For each possible input combination, there is ____ possible value for each output variable.

- ○ 5, one
- ● 32, one
- ○ 5, many
- ○ 32, many

Click **Submit** to complete this assessment.

Question **24** of **24**

Question Completion Status:

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21

⚠ Moving to another question will save this response.

Question 20

In CPU, Multiplexors are used to select certain registers to act as operands (inputs) to the _____.

- ○ Registers
- ○ Data Path
- ○ Encoder
- ● Arithmetic/Logic Unit

⚠ Moving to another question will save this response.

Remaining Time: 11 minutes, 24 seconds.

Question Completion Status:

Moving to another question will save this response.

Question 17

0.25 points

Save Answ

Considering four types of gates: AND, OR, NAND, and NOR. We have 16 combinations for first and second level gates. ____ of combinations are degenerate form

- 8
- 6
- 16
- 4

Moving to another question will save this response.

Question 17 of 24

Type here to search

28°C ENG US 9:57 4/23/2

Lenovo

PrtSc Ins

Your answers are saved automatically.

Remaining Time: 06 minutes, 09 seconds.

Question Completion Status:

1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23

⚠ Moving to another question will save this response.

Question 2

All min terms are product terms but not all product terms are min terms

- True
- False

Type here to search

emaining Time: **15 minutes, 30 seconds.**

Question Completion Status:

Prime implicant on the K-map below is

A\BC	00	01	11	10
0	1	1	1	1
1			1	1

- ○ AB
- ● A'+B
- ○ A'B'
- ○ AB+C'

⚠ Moving to another question will save this response.

Best Regards

structions

med Test This test has a time limit of 20 minutes.This test will save
Warnings appear when **half the time**, **5 minutes**, **1 min**

Multiple Attempts Not allowed. This test can only be taken once.

orce Completion Once started, this test must be completed in one sitting. D
Your answers are saved automatically.

Remaining Time: 06 minutes, 28 seconds.

Question Completion Status:

⚠ Moving to another question will save this response.

Question 20

It is impossible to implement Sum and Carry function of adder using decoder.

- ○ True
- ● False

⚠ Moving to another question will save this response.

Question 1

The value of conversion of the decimal number 394 to octal is _____.

- ○ 10011001
- ○ 107
- ☒ 612
- ○ 99

Question 2

Express the decimal number 230.41 in BCD

- ☒ 0010 0011 0000. 0100 0001
- ○ A7.DD
- ○ 00101001. 0011
- ○ 1000 0001.0101

Question 3

The function of carry in half adder

- ○ X⊕Y
- ○ X+Y
- ☒ XY
- ○ XYZ

Question 4

$(X \oplus Y)' =$

- ○ X+Y
- ○ X'Y+XY'
- ○ X'+Y'
- ☒ XY+X'Y'

Question 5

4-to-16 Decoder could be used for:

- ○ Select 16-to-1 Output
- ☒ Convert Binary to Hex
- ○ Convert Hex to Binary
- ○ Select 8-to-1 Output

Question 6

What is the name of the device below?

- ○ XOR
- ○ XNOR
- ○ OR
- ◉ NOR

Question 7

For 4 input variables the number of rows on truth table will be

- ○ 4
- ☒ 16
- ○ 32
- ○ 8

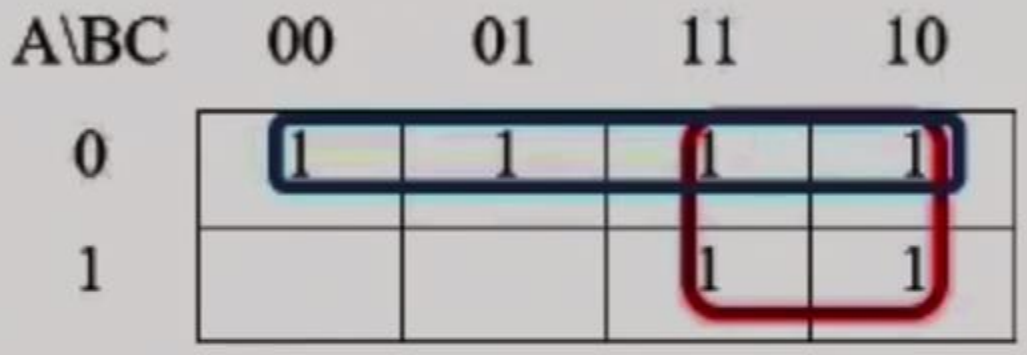
Question 8

In CPU, Multiplexors are used to select certain registers to act as operands (inputs) to the _____.

- ◉ Arithmetic/Logic Unit
- ○ Registers
- ○ Data Path
- ○ Encoder

Question 9

Prime implicant on the K-map below is



- ○ AB+C'
- ○ AB
- ○ A'B'
- ☒ A'+B

Question 10

SR latch are difficult to manage and seldom to use due to _____ condition

- ○ Wired logic
- ○ Generate
- ■ Indeterminate
- ○ Next State

Question 11

Considering four types of gates: AND, OR, NAND, and NOR. We have 16 combinations for first and second level gates. ___ of combinations are degenerate form

- ○ 16
- ○ 4
- ○ 6
- ● 8

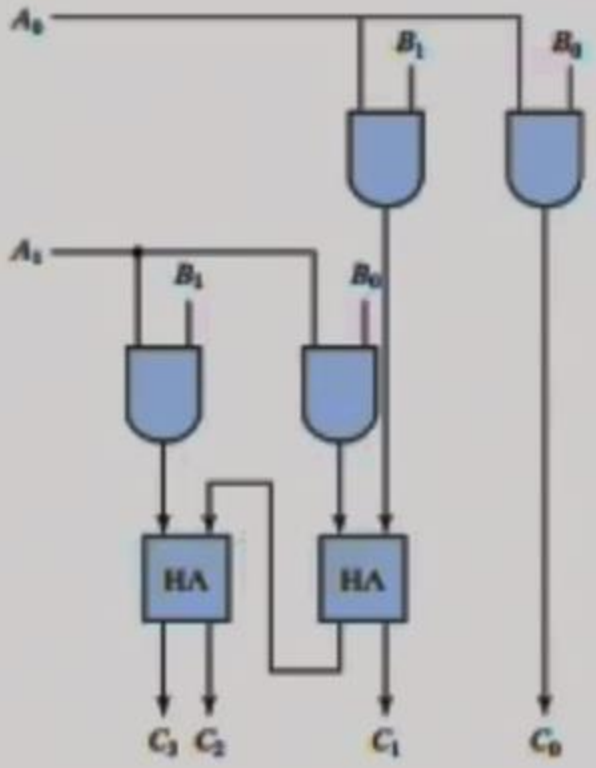
Question 12

According to the Boolean Algebra theorem X.X' and X+X is respectively equal to:

- ○ 1.X
- ○ X.1
- ○ X. X
- ■ 0.X

Question 13

The image is representing Binary multiplication:



- [x] True
- [ ] False

Question 14

Boolean algebraic functions use logic operations only

- [x] True
- [ ] False

Question 15

(X'(YZ)'W')' = (X+Y+W)(X+Z+W)

- [x] True
- [ ] False

Question 16

NAND and NOR implementations are difficult to fabricate using (CMOS Technology)

- ○ True
- ◉ False

Question 17

It is possible to optimize Mux as general purpose logic by finding relation between Function F and one input.

- ☒ True
- ○ False

Question 18

The main difference between half adder and full adder is the existence of carry as output of full adder.

- ○ True
- ◉ False

Question 19

F = A(B + C)(C + D) for such a Boolean expression. The order of evaluation is : Not => Parentheses => AND => OR

- ○ True
- ☒ False

Question 20

To obtain POS from K map, by 1. combining the 0 from the map => 2. obtain the Function from the Zeros => Applying DeMorgan theorem on the Function.

- ☒ True
- ○ False

Question 21

All min terms are product terms but not all product terms are min terms

- ☒ True
- ○ False

Question 22

It is impossible to implement Sum and Carry function of adder using decoder.

- ○ True
- ◉ False

Question 23

Digit 7 can be easily represented using Octal number system

- ☑ True
- ○ False

Question 24

In a multiplexer, the selection of a particular input line is controlled by selected lines.

- ☑ True
- ○ False

Question 11

In combinational logic, for 5 input variables there is _____ possible combination of the binary inputs. For each possible input combination, there is ____ possible value for each output variable.

- ◉ 32, one
- ○ 5, one
- ○ 32, many
- ○ 5, many

Question 12

In multiplexer, For 8 inputs we need _____ select lines.

- ○ 2
- ◉ 3
- ○ 5
- ○ 4

Question 13

In Three variable K map, four adjacent squares represent a term with one literal.

- [x] True
- [ ] False

Question 15

Storage elements that operate with signal levels are flip flops and the storage elements controlled by a clock transition are Latches

- [ ] True
- [x] False

Question 17

For four inputs Multiplexer, 2 Selector bits is needed.

- [x] True
- [ ] False

Question 20

Invert gate could be performed using 1 NAND gate with the same input.

- [x] True
- [ ] False

Question 22

Decoders and Multiplexors are mandatory components in Central Processing Unit (CPU).

- [x] True
- [ ] False

Question 23

The dual of X.0 is : X.1

- [ ] True
- [x] False

Question 18

In binary Subtractor, A-B can be done by taking only the 1's complement of B and adding it to A

- ○ True
- ● False

Question 1

If a minterm in a square is covered by only one prime implicant, that prime implicant is said to be SUM

- ○ True
- ● False

Question 2

feedback paths and memory elements are acceptable in the logic gates diagram of a sequential circuit

- ● True
- ○ False

Question 3

Gray code uses less power than BCD since it uses less transistors.

- (●) True
- ( ) False

Question 15

If number of M elements = 34, to represent the element as binary code the minimum number of bits n needed is:

- ( ) 3 Bits
- ( ) 4 Bits
- ( ) 5 Bits
- (●) 6 Bits

Question 16

In sequential circuit output state depend on:

- ○ Inputs
- ◉ Inputs and present state
- ○ Inputs and selector
- ○ Selector and Enables

Question 19

Parity Bit Checker detect errors in _____bit/s

- ◉ 3
- ○ 4
- ○ 2
- ○ 1

Question 23

Switching function F(A,B,C,D) =A'BCD'+ABCD+A'B'C'D+A'B'CD+ABC'D

- ○ Σ(2, 4, 7, 10, 11)
- ○ Σ(1, 3, 6, 13, 15)
- ○ Σ(1, 3 , 5 , 12, 14)
- ○ Σ(3, 5, 6, 9, 15)

Question 13

4-to-16 Decoder could be used for:

- ○ Convert Binary to Hex
- ○ Select 16-to-1 Output
- ○ Select 8-to-1 Output
- ○ Convert Hex to Binary

Question 2

All min terms are product terms but not all product terms are min terms

- ○ True
- ○ False

Question 17

In converting logic diagram to all NAND gates diagram, Convert all OR gates to NAND gates with _____ graphic symbols

- ○ NND
- ○ OR-NOT
- ■ NOT-OR
- ○ NOT

⚠ Moving to another question will save this response.

Question 1

Designing combinational circuit for binary subtracting can be done using Full adders and 2's complements.

- True
- False

Question 2

In a combinational circuit, the output at any time depends only on the Input value.

- (●) True
- ( ) False

Question 3

In numbering systems, 3-bits are needed to store one BCD digit.

- ○ True
- ◉ False

Question 4

The modified SR latch can eliminate the indeterminate state of the latch.

- (●) True
- ( ) False

Question 5

The regular latch will always change its stored value when the clock is enabled.

- True
- False

Question 6

When the enable signal is set to 0 in a decoder the output is affected by the input signal.

- True
- False

Question 7

When using the decoder to implement logical expression expressed as Minterms we combine the output using _____.

- ○ An OR gate
- ○ An AND gate
- ○ A combination of AND, OR gates
- ◉ A combination of AND, OR NOT gates

Question 8

When implementing a function using the multiplexer, the input to the multiplexers is connected to ether 0 or 1 which represent _____.

- ○ The values of the function
- ○ The input variables
- ● The minterms
- ○ The simplified expression values

Question 9

The Minterm m2 in a function with 3 variables is expressed as _____.

- x`y`z`
- xyz
- x`y`z
- x`yz`

Question 10

The _____ contains the input, current state, next state, output.

- ○ Truth table
- ○ K-map table
- ◉ State table
- ○ State input equations

Question 11

In subtracting two binary number with 2's complement, if there is a carry that means:

- (●) The result is positive
- ( ) The result is negative
- ( ) Nothing just discards the carry
- (●) 2's complement

Question 12

If A, B and C are the inputs of a full adder then the Sum is given by.

- ABC
- $(A \oplus B) \oplus C$
- A+B+C
- AB+CB+AC

Question 13

The value of Conversion (41)10 to binary.

- ○ $(11011)_2$
- ○ $(1101)_2$
- ◉ $(101001)_2$
- ○ $(101011)_2$

Question 14

To convert from one base to another first Convert the Integer Part, then Convert the Fraction Part, lastly _____ the two results with radix point.

- (●) sum
- ( ) multiply
- ( ) join
- ( ) divide

Question 15

A digital system consists of _____ types of circuits.

- (●) 2
- ( ) 3
- ( ) 4
- ( ) 5

:In Even parity checker, If parity was violated the Error bit should be

- Don't care ○
- 1 ●
- 0 ○
- X ○

السؤال 1

An n-bits binary code is a group of n bits that can have _____ distinct values

- $2^{n}-1$ ○
- n^{2} ○
- 2^{n} ●
- $n^{2}-1$ ○

Question 2

To use the K-map For F(V, W, X, Y, Z), we will have _____ minterms and _____squares

- ○ 16,32
- ○ 32,16
- ● 32,32
- ○ 16,16

The Boolean expression F=X'Z'+Y'Z+XY contains _____.

- 3 terms and 6 literals
- 3 terms and 9 literals
- 6 terms and 3 literals
- 9 terms and 3 literals

⚠ Moving to another question will save this response.

Question 3

The BCD code of 1234 is _____

- 0001001000110100
- 0000010011010010
- 0100001100100000
- 1110110111001011

Question 4

NAND is a Universal gate because it can emulate

- ○ NOT, AND
- ● AND, OR, NOT
- ○ NOT, OR
- ○ AND, OR

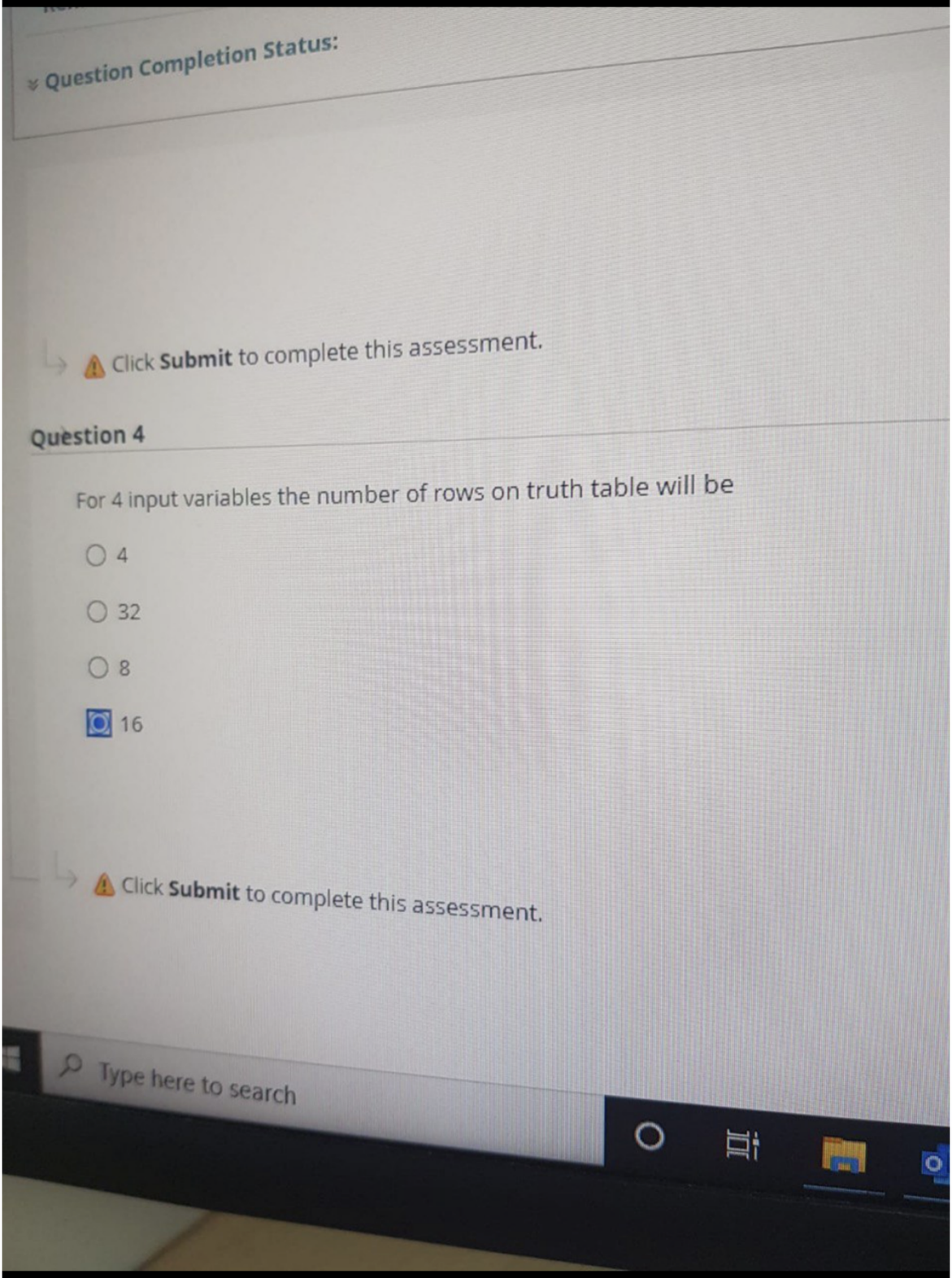
⚠ Moving to another question will save this response.

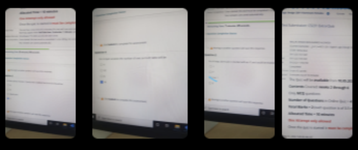
Question 1

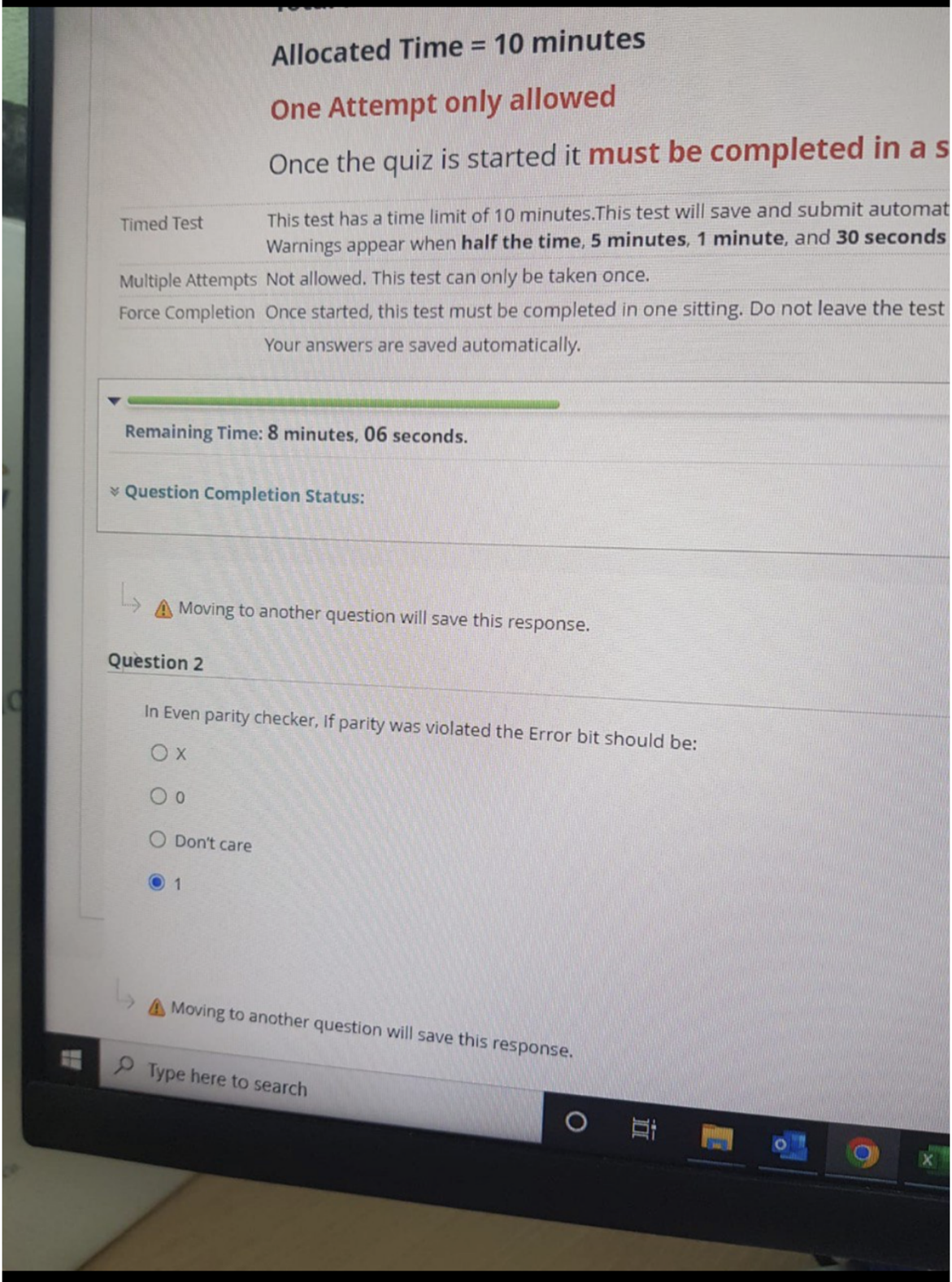
In a K map, don't care is marked with an 'X' and could be treated as

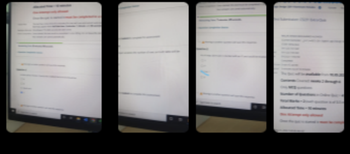
- 0 or 1
- F
- 0
- 1

⚠ Moving to another question will save this response.


Question Completion Status:
Click Submit to complete this assessment.
Question 4
For 4 input variables the number of rows on truth table will be
4
32
8
16
Click Submit to complete this assessment.
Type here to search




Allocated Time = 10 minutes
One Attempt only allowed
Once the quiz is started it must be completed in a s
Timed Test
This test has a time limit of 10 minutes.This test will save and submit automat
Warnings appear when half the time, 5 minutes, 1 minute, and 30 seconds
Multiple Attempts
Not allowed. This test can only be taken once.
Force Completion
Once started, this test must be completed in one sitting. Do not leave the test
Your answers are saved automatically.
Remaining Time: 8 minutes, 06 seconds.
Question Completion Status:
Moving to another question will save this response.
Question 2
In Even parity checker, If parity was violated the Error bit should be:
X
0
Don't care
1
Moving to another question will save this response.
Type here to search



Question 4

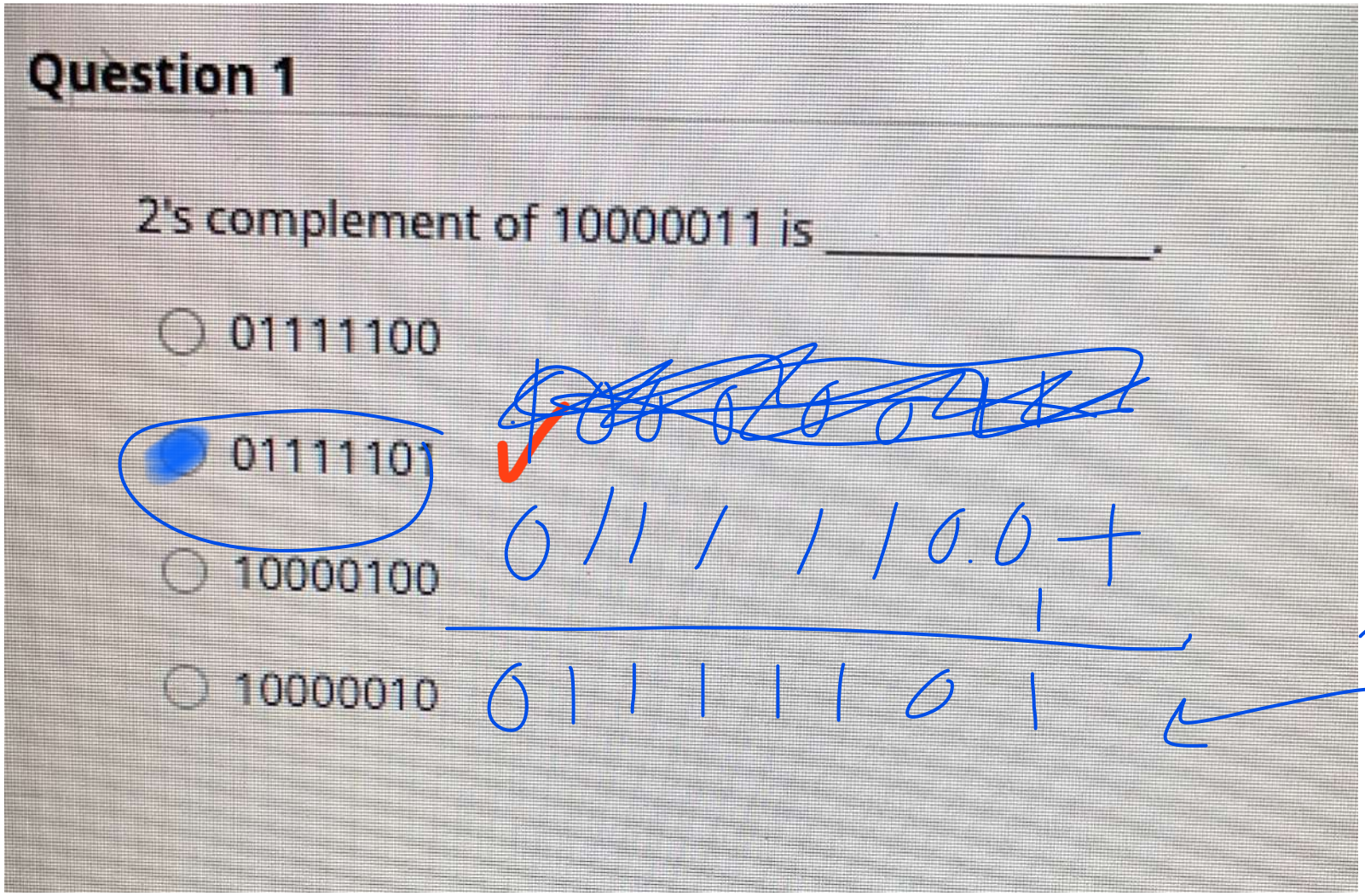
In K map, minterms m_1 is adjacent to m_3 and m_0 is adjacent to m_5 because

- ○ They have the same variable
- ○ Their minterms are identical
- ○ They have the same Gates
- ◉ Their minterms differ by one variable

Question 1

2's complement of 10000011 is _____.

- 01111100
- 0111110
- 10000100
- 10000010



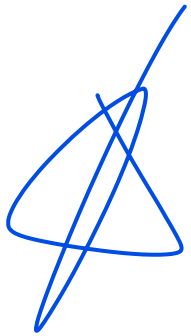
In analyzing combinational circuit, we need to make sure that the inputs is not ____

- ○ 1
- ○ Feedback
- ○ 0
- ○ Expression

Question 3

The value of Conversion (41)10 to binary.

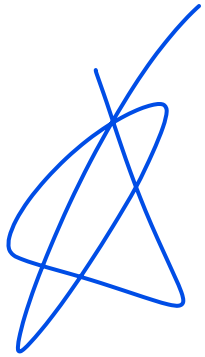
- ○ $(11011)_2$
- ○ $(1101)_2$
- ○ $(101001)_2$
- ○ $(101011)_2$

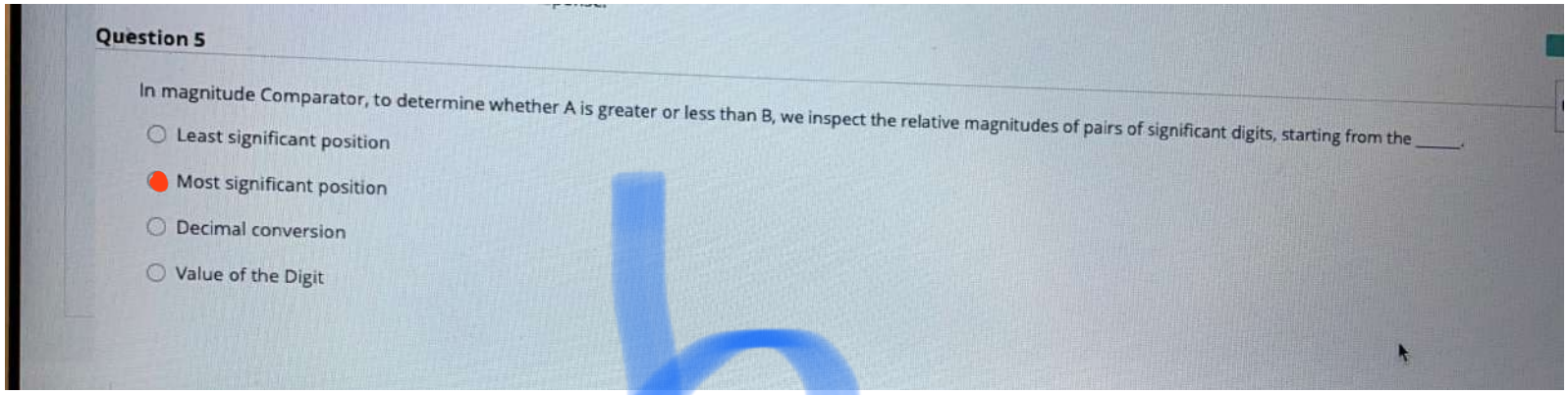


Question 4

A digital system consists of _____ types of circuits.

- 2
- 3
- 4
- 5





Question 5

In magnitude Comparator, to determine whether A is greater or less than B, we inspect the relative magnitudes of pairs of significant digits, starting from the _____.

- ○ Least significant position
- ● Most significant position
- ○ Decimal conversion
- ○ Value of the Digit

Question 6

In a combinational circuit, the output at any time depends only on the Input value.

- True
- False

Moving to another question will save this response.

Question 7

In BCD adder, the output sum cannot be greater than 9 + 9.

- ○ True
- ○ False

Question 8

A signal is a physical or virtual quantity that varies with time, or space, or another independent variable. It can be analog or digital signal.

- True
- False

Question 9

If we want to write a truth representing the following equations
F1(x,y,z) = x + x`y + z`
F2 (x,yz) = x`z+ y
We will need :

- 2 rows and 2 columns
- 3 rows and 5 columns
- 3 rows and 3 columns
- 3 rows and 6 columns

Question 10

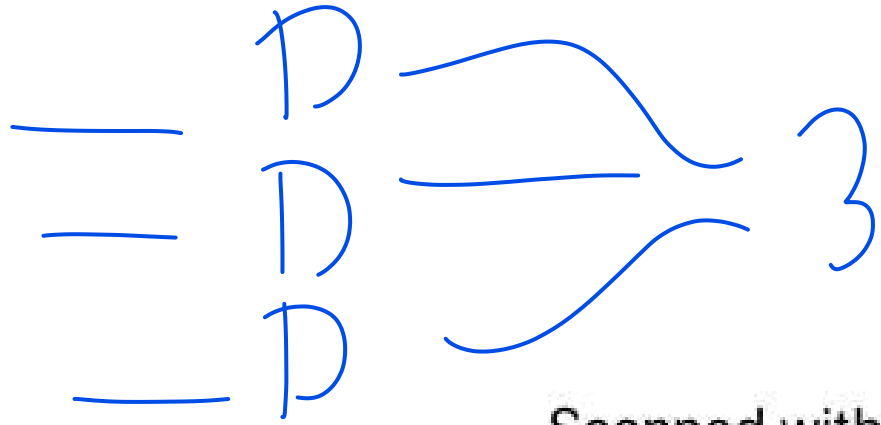
The _____ is used to determine the next value to be stored in a latch.

- ○ Input equation
- ○ Sequential equation
- ○ State value
- ○ The Q values

Question 11

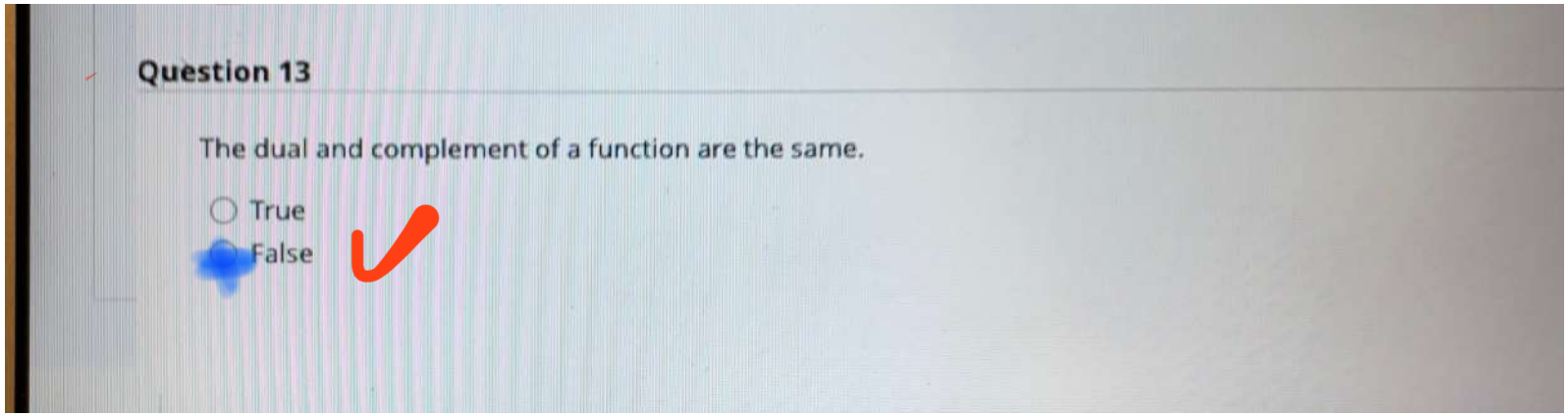
In combinational logic if we have a circuit with 4 variables for the input and 3 variables for output we can describe _____.

- 4 Boolean equations
- 3 Boolean equations
- 7 Boolean equations
- 1 Boolean equation



The expression F(A,B,C) = (A`+B+C)(A+B`+C`) is _____.

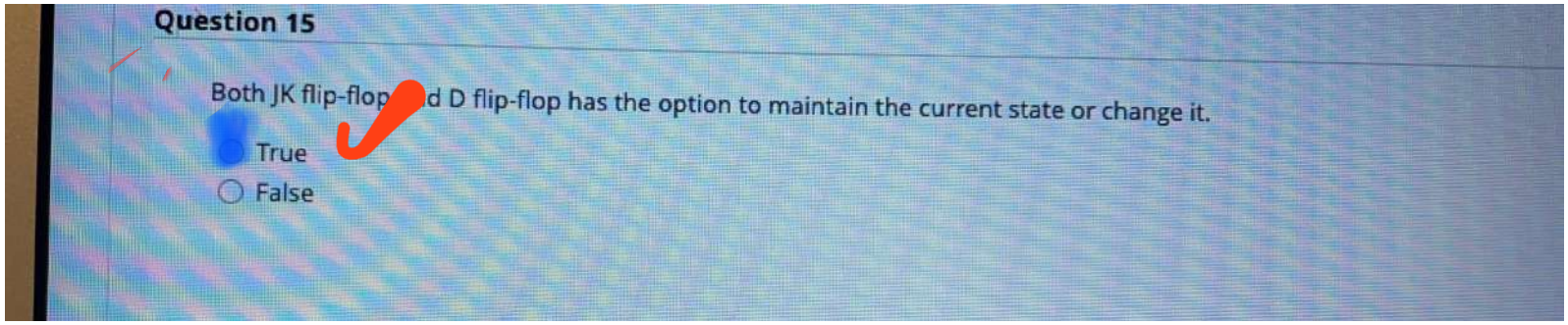
- ○ Complemented function
- ○ Sum of Minterm
- ◉ Product of Maxterms
- ○ Dual function



Question 14

The order of operation in logical expression evaluation is parenthesis, NOT, AND, OR.

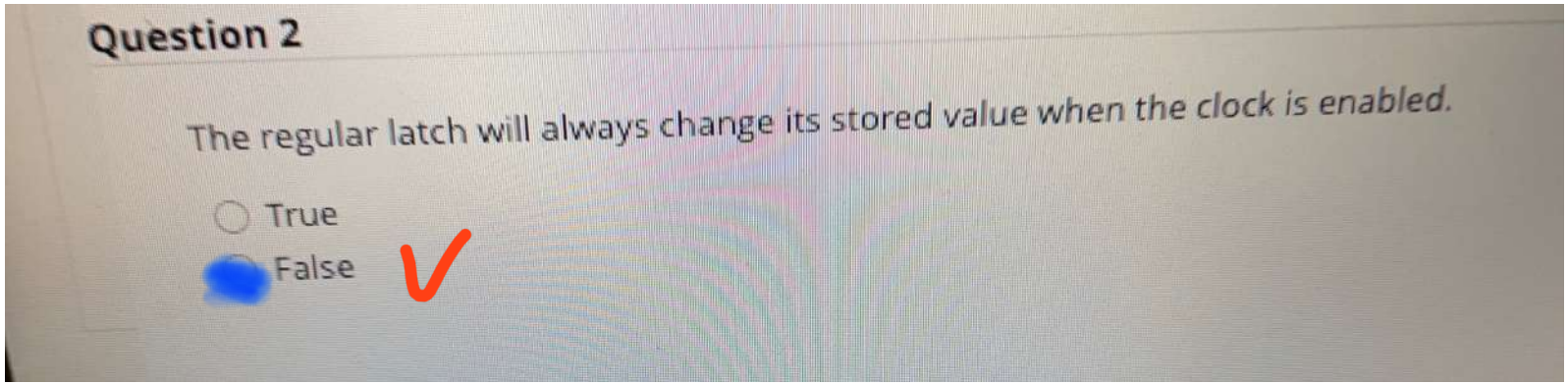
- True
- False



Question 1

In K-map we order the terms based on the binary number order.

- True
- False



Question 3

Both JK flip-flop and D flip-flop has the option to maintain the current state or change it.

- (•) True
- ( ) False

Question 4

2's complement of 10000011 is _____.

- ○ 01111100
- ○ 01111101
- ○ 10000100
- ○ 10000010

Question 5

To convert from one base to another first Convert the Integer Part, then Convert the Fraction Part, lastly _____ the two results with radix point.

- sum
- multiply
- join
- divide

Question 6

_____ principle is technique for reducing the carry propagation time in a parallel adder.

- ○ Full Adder
- ● Carry lookahead logic ✓
- ○ Half Adder
- ○ Propagation Delay

Question 7

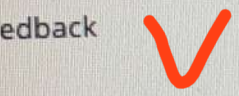
A digital system consists of _____ types of circuits.

- 2
- 3
- 4
- 5

Question 8

In analyzing combinational circuit, we need to make sure that the inputs is not _____ .

- 1
- Feedback
- 0
- Expression



Question 9

A register with 4 cells can store any discrete quantity of information that contains 32 bits.

- ○ True
- ○ False

Question 10

Digital signal (Binary) values can be represented only by digits 0 and 1.

- True
- False

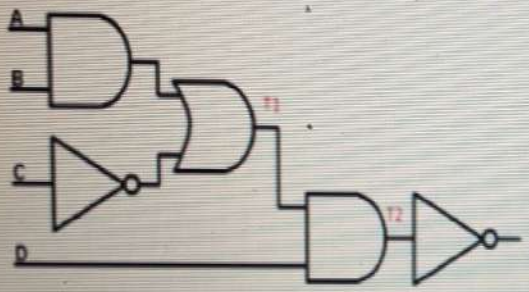
Question 11

Combinational circuit can be analyzed manually by finding the Boolean functions or truth table.

- (●) True
- ( ) False

Question 12

In the following circuit diagram what is the intermediate function T1?



- ○ AB+C
- ○ (AB)`+C`
- ○ (AB+C`)(D)
- ○ AB+C`

Question 13

In combinational logic if we have a circuit with 4 variables for the input and 3 variables for output we can describe _____.

- 4 Boolean equations
- 3 Boolean equations
- 7 Boolean equations
- 1 Boolean equation

⚠ Moving to another question will save this response.

Question 14

When using the decoder to implement logical expression expressed as Minterms we combine the output using _____.

- An OR gate
- An AND gate
- A combination of AND, OR gates
- A combination of AND, OR NOT gates

Question 15

When implementing a function using the multiplexer, the input to the multiplexers is connected to ether 0 or 1 which represent _____.

- The values of the function
- The input variables
- The minterms
- The simplified expression values

Question 1 — 0.2 points — Saved

In _____ the output depends only on the states.

- ○ Mealy model
- ● Moore model
- ○ Sequential model
- ○ Combinational

⚠ Moving to another question will save this response. Question 1 of 15

Question 2 — 0.2 points — Saved

When implementing a function using the multiplexer, the input to the multiplexers is connected to ether 0 or 1 which represent _____.

- ● The values of the function
- ◉ The input variables
- ○ The minterms
- ○ The simplified expression values

⚠ Moving to another question will save this response. Question 2 of 15

Question 3 — 0.2 points — Save Answer

The _____ is used to determine the next value to be stored in a latch.

- ○ Input equation
- ○ Sequential equation
- ○ State value
- ● The Q values

Question 4 — 0.2 points — Save Answer

The simplified expression for the function represented by the following k-map is:

- ○ wx
- ● y`z`
- ○ w`xz
- ○ wxy

Question 5 — 0.2 points — Save Answer

A register with 4 cells can store any discrete quantity of information that contains 32 bits.

- ◉ True
- ● False

⚠ Moving to another question will save this response. Question 5 of 15

⚠ Moving to another question will save this response. Question 7 of 15

Question 7 — 0.2 points — Saved

Half adders cannot add the carry bit resulting from the addition of previous bits.

- ● True
- ◉ False

⚠ Moving to another question will save this response. Question 6 of 15

Question 6 — 0.2 points — Saved

To add two binary numbers of 4 bits, Binary Adder could be used with Chain of (1) half adder and (3) full adders.

- ◉ True
- ● False

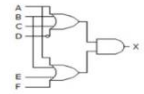
Question 10 — 0.2 points — Save Answer

If A, B and C are the inputs of a full adder then the Sum is given by.

- ○ ABC
- ● (A ⊕ B)⊕ C
- ○ A+B+C
- ◉ AB+CB+AC

Question 11 — 0.2 points — Saved

Which of the following logic expressions represents the logic diagram shown?



- (A+B+C+D')(A+B+E+F)
- ABCD'+ABEF
- ABCD
- ABEF

Question 12 — 0.2 points — Saved

Absorption theorem state that X+XY=

- X+Y
- Y
- X(X+Y)
- X

Moving to another question will save this response.

Question 13 of 15

Question 13 — 0.2 points — Save Answer

The don't care conditions can be considered 0 when working with Maxterms.

- True
- False

Moving to another question will save this response.

Question 13 of 15